Listing of Claims for Allowance:

1. (Previously presented) An apparatus for converting data between serial and parallel formats, comprising:

one or more serial data channels;

a storage element associated with each of said one or more serial data channels and having at least first and second arrays of storage cells, wherein each of said storage cells includes first and second ports, wherein the first ports of all storage cells of a storage element are connected in parallel to a data bus interconnecting the storage element with an associated channel, and wherein the data bus comprises at least one buffering element arranged to separate said data bus into portions, each of said portions being connected to the first port of at least one of said storage cells of each array of said storage element; and

means for enabling data transfer between said bus and at least one of said storage cells via a corresponding one of said first ports, and for enabling data transfer from at least one of said portions to an adjacent portion via said at least one buffering element.

2. (Previously presented) An apparatus as claimed in claim 1, wherein said means for enabling data transfer comprises first clock generating means adapted to control access to said storage cells and to control the data transfer to the adjacent portion.

3. (Previously presented) An apparatus as claimed in claim 2, wherein said first clock generating means is adapted to a transmission speed corresponding to an associated said serial data channel.

4. (Previously presented) An apparatus as claimed in any preceding claim, wherein the first ports of the storage cells of each of said arrays are adapted to be accessed sequentially.

5. (Previously presented) An apparatus as claimed in claim 1, wherein said buffering element includes at least one side, and for each of said arrays, the first ports of the storage cells are disposed on each side of the buffering element and are adapted to be accessed simultaneously.

6. (Previously presented) An apparatus as claimed in claim 1, wherein said buffering element comprises a pipeline register.

7. (Previously presented) An apparatus as claimed in claim 1, wherein the second ports of each of said storage cells are connected in parallel across all of said arrays.

8. (Previously presented) An apparatus as claimed in claim 2, further comprising means for controlling access to the storage cells of one of said array simultaneously via said second ports.

9. (Previously presented) An apparatus as claimed in claim 8, wherein said means for controlling access to the storage cells comprises a second clock generating means.

10. (Previously presented) An apparatus as claimed in claim 1, wherein said storage cells comprise dual-port random access memory (RAM) cells.

11. (Previously presented) An apparatus as claimed in claim 1, wherein each of said arrays is adapted to store at least one data packet.

12. (Previously presented) An apparatus as claimed in claim 1, wherein each of said arrays is adapted to store part of a data packet.

13. (Previously presented) An apparatus as claimed in claim 1, wherein said storage cells are arranged to store more than one bit of data simultaneously.

14. (Previously presented) An apparatus as claimed in claim 1, wherein said data is converted from a serial to parallel format and wherein said first ports are input ports and said second ports are output ports.

15. (Previously presented) An apparatus as claimed in claim 1, wherein said data is converted from a parallel to serial format and wherein said first ports are output ports and said second ports are input ports.

16. (Previously presented) An apparatus for converting data input through at least one channel in a serial format into a parallel format, comprising:

at least one serial data input channel;

a storage element associated with each said serial data channel and having at least first and second arrays of storage cells, wherein each of the storage cells includes an input port and an output port, such that input ports for all of the storage cells of the storage element are connected in parallel to a data bus interconnecting the storage element with an associated serial data channel, and wherein said data bus comprises at least one buffering element arranged to separate said data bus into portions, each of said portions being connected to an input port of at least one of said storage cells of each array of said storage element; and

means for enabling data input from said data bus to at least one of said storage cells in said storage element and for enabling said buffering element to buffer said data onto said data bus portion in accordance with a predetermined input cycle.

17. (Previously presented, and to be restored) An apparatus for converting data from a parallel format into a serial format, comprising:

at least one serial data output channel;

a storage element associated with each said serial data output channel and having at least first and second arrays of storage cells, each of the storage cells including an input port and an output port, such that output ports for all of the storage cells of the storage element are connected in parallel to a data bus interconnecting the storage element with an associated serial data output channel, and wherein said data bus comprises at least one buffering element arranged to separate said data bus into portions, each of said portions being connected to an output port of at least one of said storage cells of each array of said storage element; and

means for enabling data output from at least one of said storage cells in said storage element onto said data bus and for enabling said buffering element to the buffer said data onto data bus portion in accordance with a predetermined output cycle.

18. (Previously presented) A method for converting serial data to a parallel format utilising an apparatus for converting data between serial and parallel formats, said apparatus comprising one or more serial data channels; a storage element associated with each of said serial

data channels and having at least first and second arrays of storage cells, wherein each of said storage cells includes first and second ports, wherein the first ports of all storage cells of a storage element are connected in parallel to a data bus interconnecting the storage element with an associated channel, and wherein the data bus comprises at least one buffering element arranged to separate said data bus into portions, each of said portions being connected to the first port of at least one of said storage cells of each array of said storage element; and means for enabling data transfer between said bus and at least one of said storage cells via a corresponding one of said first ports, and for enabling data transfer from at least one of said portions to an adjacent portion via said at least one buffering element, said method comprising the steps of:

transmitting serial data from each of said channels onto the said data bus associated therewith, and

enabling sequential input of data from the data bus into said storage cells of a corresponding one of said arrays for each of said storage elements in accordance with a write cycle.

19. (Previously presented) A method as claimed in claim 18, further comprising the step of, simultaneous with the step of enabling sequential input of data, outputting data from the storage cells of the other of said arrays for each storage element sequentially and in accordance with a read cycle.

20. (Previously presented) A method as claimed in claim 19, further comprising the step of splitting the outputting of data from the storage cells over at least two read cycles.

21. (Previously presented) A method as claimed in claim 18 further comprising the step of enabling data transfer from one of said bus portions to an adjacent bus portion during each said write cycle.

22. (Previously presented) A method as claimed in claim 21, further comprising the step of commencing the sequential input of data into each of said arrays from one of the portions arranged furthest from an associated serial data channel.

23. (Previously presented) A method as claimed in claim 22, further comprising the step

of enabling the sequential input of data to the storage cells at an end of one of said bus portions and at a beginning of a next bus portion simultaneously.

24. (Previously presented) A method as claimed in claim 18, further comprising the step of adapting the write cycle for each said storage element to be at a transmission speed of an associated serial data channel.

25. (Previously presented) A method as claimed in claim 19, further comprising the step of adapting the read cycle to correspond to a total bandwidth of every said channel.

26. (Previously presented, and to be restored) A method for converting parallel data to a serial format utilizing an apparatus as claimed in any one of claims 1 or 17, said method comprising the steps of:

enabling the sequential output of data from the storage cells of one of said arrays for each storage element onto the data bus in accordance with a read cycle; and

transmitting serial data from the data bus onto the serial data channel associated therewith.

27. (Previously presented, and to be restored) A method as claimed in claim 26, further comprising the step of, simultaneous with the step of enabling the sequential output of data, inputting data into the memory cells of the other of said arrays for each storage element sequentially and in accordance with a write cycle.

28. (Previously presented, and to be restored) A method as claimed in claim 27, further comprising the step of splitting the inputting of data into the storage cells of one array over at least two write cycles.

29. (Previously presented, and to be restored) A method as claimed in claim 26, further comprising the step of enabling data transfer from one of said bus portions to an adjacent bus portion during each said write cycle.

30. (Previously presented, and to be restored) A method as claimed in claim 29, further comprising the step of commencing the output of data from each of said arrays onto one of the

portions arranged closest to an associated serial data channel.

31. (Previously presented, and to be restored) A method as claimed in claim 30, further comprising the step of enabling the sequential output of data from the storage cells at an end of one of said bus portions and at a beginning of a next bus portion simultaneously.

32. (Previously presented, and to be restored) A method as claimed in claim 26, further comprising the step of adapting the read cycle for each said storage element to be at a transmission speed of an associated serial data channel.

33. (Previously presented, and to be restored) A method as claimed in claim 27, further comprising the step of adapting the write cycle to correspond to a total bandwidth of every said channel.

34. (Previously presented) A communications switch comprising said apparatus as claimed in any one of claims 1 or 16.

35. (Previously presented) A communications switch comprising said method as claimed in claim 18.

Amendments to the Drawings:

The attached sheets of drawings include changes to FIG. 1-6. As shown on the attached annotated sheets, the amendment adds clarifying text as requested by the Examiner and correct minor typographical errors. No new matter has been added.

The Amendments to the Drawings are being filed simultaneously with the submission of formal drawings incorporating the proposed changes. The formal drawings include the Replacement Sheets.

Attachments: Annotated Sheets Showing Changes.
(Replacement Sheets are being filed simultaneously as part of the submission of formal drawings incorporating the proposed changes.)